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09/398,689	09/20/1999	ARMIN MRASEK	GR98P2610	1397

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 03/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/398,689	Applicant(s) MRASEK, ARMIN	
	Examiner Christopher E. Lee	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 10th of February, 2003. No claims has been amended; no claims has been canceled; and no claims has been newly added. Currently, claims 1-6 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [hereinafter AAPA] in view of Ugajin et al. [JP 363292747 A; hereinafter Ugajin].

Referring to claim 1, AAPA discloses an improved method for transmitting digital data divided up into data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled by a microprocessor (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC receiver), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line 1); reading via said microprocessor said digital data from said memory (See page 2, lines 11-12; i.e., wherein in fact that a microprocessor removes the data contained in the FIFO memory implies that said microprocessor reads said digital data from said memory); and transmitting from said microprocessor to said memory control unit an acknowledgment of a reception of a data block of said digital data (See Fig. 6A and B).

AAPA does not disclose said memory having a settable size; determining via said microprocessor from said memory control unit a quantity of said digital data to be read from said memory; and setting via said microprocessor a size of said memory.

Ugajin discloses a buffer management system, wherein a memory (reception buffer 78b of Fig. 2) having a settable size (See page 282, paragraph right-top, lines 7-16); determining (decision block in Fig. 3) via a microprocessor (means for running software sequence in Fig. 3; See page 283, paragraph left-top, lines 3-6 and paragraph left-bottom, lines 2-6) from a memory control unit (LLC protocol controller 67 of Fig. 2) a quantity of digital data to be read from said memory (i.e., traffic flow of receiving data; See Fig. 5 and page 283, paragraph left-bottom, lines 19-20); and setting (See block for "setting reception buffer length on the traffic buffer ratio table" in Fig. 3) via said microprocessor (i.e., means for running software sequence in Fig. 3) a size (i.e., new reception buffer length) of said memory (i.e., reception buffer). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of managing reception buffer, as disclosed by Ugajin, in said method for transmitting digital data, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., reception buffer size; See page 281, paragraph right, lines 1-5 of Ugajin).

Referring to claim 2, AAPA discloses supplying said digital data from said first data bus (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) which checks whether said digital data has been received correctly (See page 1, line 25 through page 2, line 1 and lines 7-9; i.e., wherein in fact HDLC control device checks the data protection information implies that said HDLC logic unit checks whether said digital data has been received correctly) before said digital data is written to said memory (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC receiver logic unit implies that said digital data (i.e., HDLC signal) has been received before said digital data is written to said memory).

Referring to claim 5, AAPA discloses a configuration (i.e., network interface equipment for ISDN; See page 1, lines 25-26) for transmitting digital data divided up into data frames of variable length from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled and read by a microprocessor (See the preamble of claim 1 in a Jepson-type claim, which is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said configuration comprising: a memory (i.e., a FIFO memory) having a fixed size for storing data received from said first data bus (See page 2, line 9-12); a control device (i.e., HDLC receiver) for controlling access operations (i.e., informing said microprocessor, in a form of an interrupt generated by said control device; See page 9, line 24 through page 10, line 1) to said memory by said first data bus and said microprocessor (See Fig. 6A and 6B).

AAPA does not disclose said memory having a variable size; and a first, a second registers.

Ugajin discloses a buffer management system, wherein a memory (reception buffer 78b of Fig. 2) having a variable size (See page 282, paragraph right-top, lines 7-16); a first register (initial setting value table 74 of Fig. 4) storing a value (reception buffer length 73 of Fig. 4) representing a present size of said memory (i.e. reception buffer), said value being variable in each read cycle of said microprocessor (See Fig. 3 and page 284, paragraph right-bottom, lines 2-9); and a second register (transmission/reception buffer ratio table 80 of Fig. 5) storing a quantity of said data just written to said memory (i.e., traffic flow of receiving data; See Fig. 5 and page 283, paragraph left-bottom, lines 19-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic buffer management system, as disclosed by Ugajin, in said configuration, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., reception buffer size; See page 281, paragraph right, lines 1-5 of Ugajin).

Referring to claim 6, AAPA discloses a high-level data link control HDLC logic unit (i.e., HDLC control device) connected between said first data bus and said memory (See page 2, lines 7-11).

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Ugajin [JP 363292747 A] and Chee et al [US 5,673,416; hereinafter Chee].

Referring to claim 3, AAPA discloses an improved method for transmitting digital data divided up into data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to said first data bus (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); and informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC receiver), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line 1).

AAPA does not disclose said memory having a settable size.

Ugajin teaches a buffer management system, wherein a memory (reception buffer 78b of Fig. 2) having a settable size (See page 282, paragraph right-top, lines 7-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said reception buffer, as disclosed by Ugajin, for said memory, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., reception buffer size; See page 281, paragraph right, lines 1-5 of Ugajin).

AAPA, as modified by Ugajin, does not disclose performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data from said first data bus, and said microprocessor asking said memory control unit if said memory is ready

to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory.

Chee discloses a memory request and control unit, wherein performing one of informing a microprocessor (display FIFO module 12 of Fig. 2), in a form of interrupt (i.e., DispDataAck from DRAM controller sequencer 22 to display FIFO module 12 in Fig. 3) generated by a memory control unit (DRAM controller sequencer 22 of Fig. 3), if a memory (DRAM 24 of Fig. 3) is ready to accept new data (See col. 9, lines 20-23), and said microprocessor (i.e., display FIFO module) asking (i.e., a low priority request DispLoReq in Fig. 3) said memory control unit (i.e., DRAM controller sequencer) if said memory is ready to accept said new data. (See col. 10, lines 55-57); writing via said microprocessor said new data to said memory (See col. 9, lines 58-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of memory request and control unit, as disclosed by Chee, in said method, as disclosed by AAPA, as modified by Ugajin, for the advantage of utilizing simple circuit for said microprocessor (i.e., display FIFO module) for efficiently determining when to issue requests for said memory (i.e., DRAM access; See col. 2, lines 41-43 of Chee).

AAPA, as modified by Ugajin and Chee, discloses performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data from said first data bus, and said microprocessor asking said memory control unit if said memory is ready to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory; setting (See block for "setting reception buffer length on the traffic buffer ratio table" in Fig. 3; Ugajin) via said microprocessor (i.e., means for running software sequence in Fig. 3; Ugajin) a size (i.e., new reception buffer length; Ugajin) of said memory (i.e., reception buffer; Ugajin); transmitting from said microprocessor to said memory control unit an acknowledgment of an end of transmission of said new data (See Fig. 6A and B); and placing said new data onto said second data bus (i.e., transmitting

digital data (i.e., new data) to a second data bus; See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*).

Referring to claim 4, AAPA discloses supplying said new data (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) before it is placed onto the second data bus (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC receiver logic unit implies that supplying said new data (i.e., HDLC signal) to a high-level data link control logic unit before it is placed onto the second data bus), said high-level data link control logic unit adding error-checking data (i.e., adding protection information) to said new data (See page 2, lines 16-18).

Response to Arguments

5. The Applicant states the arguments with the reference 'JP 262 191 747 A' in Response filed on 10th of February, 2003 (hereinafter Response), which had not been brought to the claim rejections in the prior Office Action mailed on 6th of November, 2002 (hereinafter 'prior Office Action'). The Examiner brought the references Applicant Admitted Prior Art, Ugajin et al. [JP 363292747 A] and Chee et al [US 5,673,416] for the prior art rejections. However, the Examiner assumes the reference 'JP 262 191 747 A' could be the reference 'JP 363 292 747 A' because the Applicant admits the Examiner rejected the claims 1, 2, 5, and 6 as being obvious over Applicant's admitted prior art in view of Ugajin et al (JP 363292747 A) under 35 U.S.C. § 103 (See the Response, page 2, lines 22-25), for the purpose of Examiner's Response to Applicant's Argument.

6. *In response to the Applicant's argument with respect to* "The Examiner has the opinion that the prior art timing diagrams shown in Fig. 6A and 6B of the application disclose the claimed invention except for the portions that have been underlined above. ... Applicant believes that one does not obtain a suggestion to incorporate the features that are not taught in Fig. 6A and 6B merely by referring to JP 363 292 747 A" on the Response, page 4, line 20 through page 5, line 7, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, the Examiner described that the limitation "transmitting digital data divided up into data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled by a microprocessor" in the preamble of the claims 1 and 3 is taught as a Prior Art in their preambles, respectively, since the claims 1 and 3 are, respectively, using Jepson-Type claim (See the preamble of these claim, which are Jepson-type claim, is impliedly admitted to be old in the art; See M.P.E.P. 2129 *Admission as Prior Art*). And, the same limitation in the preamble of the claim 5 is also taught by the preamble limitation in the claims 1 and 3, which is impliedly admitted to be old in the art. Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the claims 1 and 5 rejections under *35 USC §103(a)* in the prior Office Action are established a *prima facie* case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001), and the Examiner has clearly pointed out rationale for appropriate combination of the references. See the prior Office Action, page 2, Paragraph 3, claims 1and 5 rejections under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Ugajin. Thus, the Applicant's argument on this point is not persuasive.

7. *In response to the Applicant's argument with respect to* "Claims 1 and 5 respectively define a method a configuration for ISDN data transmission in which the size of the intermediate storage is adapted to the data packets that will be transmitted for the purpose of efficient and rapid data communication. ... Particularly, the adjustable memory would also have to be designed for the transmission of the fixed data packets, as they are common in ISDN standard." on the Response, page 5, lines 8-25, the Examiner respectfully disagrees. According to the Applicant's statement, it is noted that

the features upon which applicant relies (i.e., claims 1 and 5 respectively define a method and a configuration for ISDN data transmission) are not recited in the rejected claims 1 and 5. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In other words, the Applicant's argument based upon the features, such that ISDN data transmission and ISDN standard, which are not recited in the claims 1 and 5, respectively, alludes to elements beyond the scope of the Applicant's claimed invention. Thus, the Applicant's argument on this point is not persuasive.

8. *In response to the Applicant's argument with respect to* "This document (i.e., JP 363 292 747 A) discloses a buffer memory device with a memory size that can be variably adjusted. ... JP 363 292 747 A merely describes variably partitioning an intermediate storage device between a transmission device and a reception device. ... An intermediate storage device according to JP 363 292 747 A for constantly structured data or even blocks of constant size, as for example in ATM systems, however, ... JP 363 292 747 A obviously pertains to a data transmission system that is similar to the ATM system. ... JP 363 292 747 A is simply not pertinent. ... Claim 3 is not obvious for the reason specified above with regard to JP 363 292 747 A." on the Response, page 6, line 2 through page 8, line 24, the Examiner respectfully disagrees. The Examiner brought Ugajin, which discloses a buffer management system to prevent the deterioration in the communication performance by changing the transmission/reception buffer rate (See Ugajin, page 281, Paragraph 2). However, the Examiner believes Ugajin (1) does not teach variably partitioning an intermediate storage device between a transmission device and a reception device, but teaches changing the transmission/reception buffer rate in memory length (i.e., memory area) in an increasing direction of the size of reception buffer when the number of times of buffer busy states read periodically exceeds a predetermined value, (2) does not teach an intermediate storage device is for constantly structured data or even blocks of constant size, as for example in ATM systems, and (3) does not teach a data transmission system obviously pertains to the ATM system. Therefore, the Applicant's

arguments based on the elements, which are not taught by the reference Ugajin used in the prior Office Action for the prior art rejections, are not pertinent to be discussed. Thus, the Applicant's argument on this point is not persuasive.

9. *In response to the Applicant's argument with respect to* "Further, applicant believes that Chee et al. (5,673,416) is nor relevant in view of the object of the instant application. ... Data management, however, does not take place here." on the Response, page 9, lines 1-15, the Examiner respectfully disagrees. The Applicant alleges that the reference Chee et al. [US 5,673,416] fails to show certain features of applicant's invention, it is noted, however, that the features upon which applicant relies (i.e., the instant application has a single priority and a data management) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, the Applicant's argument on this point is not persuasive.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

CEL/ CEL
March 12, 2003

MARK H. RINEHART
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